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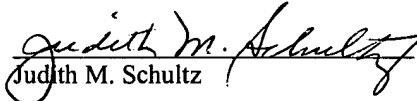
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Brian David Johansson et al.
Serial No.: 10/786,357
Confirmation No.: 4567
Filed: February 25, 2004
For: LOGIC LEVEL VOLTAGE TRANSLATOR

Examiner: Long T. Nguyen
Art Unit: 2816

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 17th day of August, 2005.


Judith M. Schultz

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

Responsive to the Office Action mailed June 20, 2005, Applicants request reconsideration of this application. To further the prosecution of the application, an election has been made.

In the Office Action, the Examiner required that this application be restricted to one of the following inventions:

- I. Claims 1-16, drawn to a voltage level translator;
- II. Claims 17-20, drawn to a ready-signal generation circuit.

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Applicants hereby elect Group I, including claims 1-16, for examination in the present application. Applicants reserve the right to file a divisional application pursuing claims 17-20 in Group II.

Respectfully submitted,
Brian David Johansson et al., Applicants


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